System and Method for Incremental Statistical Timing Analysis of Digital Circuits

ABSTRACT

The present invention is a system and method for efficiently and incrementally updating the statistical timing of a digital circuit after a change has been made in the circuit. One or more changes in the circuit is/are followed by timing queries that are answered efficiently, constituting a mode of timing that is most useful in the inner loop of an automatic computer-aided design (CAD) synthesis or optimization tool. In the statistical re-timing, the delay of each gate or wire is assumed to consist of a nominal portion, a correlated random portion that is parameterized by each of the sources of variation and an independent random portion. Correlations are taken into account. Both early mode and late mode timing are included; both combinational and sequential circuits are handled; static CMOS as well as dynamic logic families are accommodated.